

Appl. No. 10/810,023
Amdt. Dated Apr. 5, 2006
Reply to Office Action of January 5, 2006

REMARKS

Claim Rejections under 35 U.S.C. 102

Claims 1-5 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Jones et al. (U.S. 5,534,743).

As regards independent claim 1, applicants have amended this claim without any new matter being entered, and respectfully traverse the rejection for the following reasons:

Amended claim 1 recites:

A barrier array for use in a flat panel display, comprising:

a shadow mask including a plurality of openings defined therethrough according to a predetermined pattern, the predetermined pattern being in accordance with a pixel pattern of a flat panel display, the shadow mask having an upper surface and a lower surface; and

an insulative layer including a first portion formed on the upper surface of the shadow mask and a plurality of second portions extending from the upper surface to the lower surface through the respective openings.

Applicants submit that neither Jones '743 nor any of the other cited references, alone or in combination, discloses, teaches, or otherwise suggests the invention as currently set forth in claim 1.

Jones '743 does disclose a gate electrode for use in a field emitter structure. As illustrated in FIG 7, the gate electrode is a metal layer 28

formed on a first etch dielectric material layer 26. A second etch dielectric material layer 30 is formed on the metal layer 28 (see column 6, lines 9-17). The metal layer 28 has a plurality of openings according to a predetermined pattern, but the openings are formed via differential etching after the first etch dielectric material layer 26, the metal layer 28 and the second etch dielectric material layer 30 having been formed in that order. **Therefore, a plurality of inner side surfaces bounding the respective openings and adjoining the first etch dielectric material layer 26 and the second etch dielectric layer 28 are not covered by the dielectric material layer 30.** In addition, Jones '743 does disclose a layered dielectric spacer 90 and a spacer assembly 98. As illustrated in FIG. 9, the spacer assembly 98 comprises a three-layer spacer assembly including a top spacer 100, an intermediate spacer 102 and a bottom spacer 104 (column 11, lines 14-19). **However, the layered dielectric spacer 90 and the spacer assembly 98 are both selected from suitable dielectric materials.**

Therefore Jones '743 does not disclose, teach or suggest the barrier array comprising: a shadow mask including a plurality of openings defined therethrough according to a predetermined pattern, the predetermined pattern being in accordance with a pixel pattern of a flat panel display, **the shadow mask having an upper surface and a lower surface; and an insulative layer including a first portion formed on the upper surface of the shadow mask and a plurality of second portions extending from the upper surface to the lower surface through the respective openings.** Accordingly, Jones '743 clearly fails to disclose, teach or suggest the present invention as set forth in amended claim 1.

In addition, the structure of the barrier array of the present invention

produces new and unexpected results as follows. Referring to para. [0025], making a shadow mask is a known technology in CRTs which has high precision. Thus the barrier array of the present invention is convenient to make. In addition, the thickness and the material of the insulative layer can be determined according to the insulative performance required for the field emission display. Therefore, the present invention provides a barrier array having high precision and low production costs.

In summary, applicants submit that amended claim 1 is not only novel over Jones '743 under s.102, but is also unobvious over Jones '743 under s.103. Accordingly, claims 2-5 which depend from claim 1 should also be patentable over Jones '743 under U.S.C. 102 and 103. Reconsideration and withdrawal of the rejection and allowance of claims 1-5 are respectfully requested.

As regards claim 18, applicants have amended this claim without any new matter being entered. Applicants respectfully traverse the rejection of claim 18 for the following reasons:

Amended claim 18 recites:

A barrier array for use in a flat panel display, comprising:

a metal plate including a plurality of openings therethrough according to a pixel pattern of a flat panel display, the metal plate having an upper surface and a lower surface; and

an insulative layer including a first portion formed on the upper surface of the metal plate and a plurality of second portions extending from the upper surface to the lower surface through the respective openings.

Jones '743 does disclose a gate electrode for use in a field emitter structure. As illustrated in FIG 7, the gate electrode is a metal layer 28 that is formed on a first etch dielectric material layer 26. A second etch dielectric material layer 30 is formed on the metal layer 28 (see column 6, lines 9-17). The metal layer 28 has a plurality of openings according to a predetermined pattern, but the openings are formed via differential etching after the first etch dielectric material layer 26, the metal layer 28 and the second etch dielectric material layer 30 having been formed in that order. Thus a plurality of inner side surfaces bounding the respective openings and adjoining the first etch dielectric material layer 26 and the second etch dielectric layer 28 are not covered by the dielectric material layer 30.

Therefore Jones '743 does not disclose, teach or suggest: a metal plate including a plurality of openings therethrough according to a pixel pattern of a flat panel display, the metal plate having an upper surface and a lower surface; and an insulative layer including a first portion formed on the upper surface of the metal plate and a plurality of second portions extending from the upper surface to the lower surface through the respective openings. Accordingly, Jones '743 clearly fails to disclose, teach or suggest the present invention as set forth in amended claim 18.

In addition, the structure of the barrier array of the present invention produces new and unexpected results as follows. Referring to para. [0025], making a shadow mask is a known technology in CRTs which has high precision. Thus the barrier array of the present invention is convenient to make. In addition, the thickness and the material of the insulative layer can be determined according to the insulative

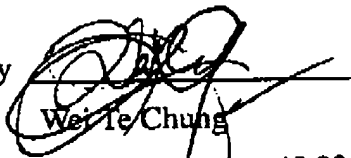
performance required for the field emission display. Therefore, the present invention provides a barrier array having high precision and low production costs.

In summary, applicants submit that amended claim 18 is not only novel over Jones '743 under s.102, but is also unobvious over Jones '743 under s.103. Reconsideration and withdrawal of the rejection and allowance of claim 18 are respectfully requested.

In view of the foregoing, the present application as claimed in the pending claims is considered to be in a condition for allowance, and an action to such effect is earnestly solicited.

Respectfully submitted,
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By



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